09/935,939 IBM/67DV1

predetermined penalty in response to a write to a block of data associated with said counter.

Remarks

Applicant is proposing an amendment to claims 51 and 52 for the purposes of appeal, to eliminate the duplication of the word "wherein" in those claims. Applicant submits that this is correcting an obvious typographical error and requests entry.

If any petition for extension of time is necessary to accompany this communication, please consider this paper a petition for such an extension of time, and apply the appropriate extension of time fee to Deposit Account 23-3000. If any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

Thomas W. Humphrey Reg. No. 34,353

Let Le

Wood, Herron & Evans, L.L.P. 2700 Carew Tower 441 Vine Street Cincinnati, OH 45202-2917

Voice: (513) 241-2324 Facsimile: (513) 241-6234 09/935,939 IBM/67DV1

Version With Markings to Show Changes Made

51. The cache control circuit of claim 50 wherein [wherein] said control circuit maintains statistics on types of accesses made to data by maintaining a counter associated with blocks of data, said counters being credited or penalized in response to types of accesses made to the associated block of data.

52. The cache control circuit of claim 51 wherein [wherein] said control circuit maintains statistics by crediting a counter by a predetermined credit in response to a read to a block of data associated with said counter, and penalizing said counter by a predetermined penalty in response to a write to a block of data associated with said counter.